CLAIMS

What is claimed is:

1. A method comprising:

reading a time of exiting a reduced power consumption state prior to an execution of an interrupt routine;

storing the time of exiting the reduced power consumption state in a register; and

calculating a reduced power consumption state duration based on the time of exiting the reduced power consumption state stored in the register.

2. The method of claim 1 wherein the reduced power consumption state is a C1 power state.

3. The method of claim 1 further comprising:

reading a time of entering the reduced power consumption state;

storing the time of entering the reduced power consumption state in a main memory; and

calculating the reduced power consumption state duration utilizing the time of entering and the time of exiting the reduced power consumption state.

4. The method of claim 1 wherein the register is located in a chipset.

5. The method of claim 1 wherein the register is located in a processor.

6. A method comprising:

starting a time counter;

entering a reduced power consumption state;

halting the time counter prior to an execution of an interrupt routine; and

exiting the reduced power consumption state.

7. The method of claim 6 wherein the starting the time counter comprises requesting a chip to start a time counter.

8. The method of claim 6 wherein the halting the time counter comprises requesting a chip to halt the time counter.

9. The method of claim 7 wherein the chip is a personal computer chipset.

10. The method of claim 8 wherein the chip is a personal computer chipset.

11. The method of claim 6 wherein the exiting the reduced power consumption state comprises executing the interrupt routine.

12. The method of claim 6 wherein the time counter comprises a reduced power consumption state duration.

13. The method of claim 6 wherein the reduced power consumption state is a C1 power state.

14. A method comprising:

storing a time of entering a reduced power consumption state in a chip;

storing a time of exiting the reduced power consumption state in the chip prior to an execution of an interrupt routine; and

automatically calculating a reduced power consumption state duration.

15. The method of claim 14 wherein the storing the time of entering the reduced power consumption state comprises storing the time of entering in a register.

16. The method of claim 14 wherein the storing the time of exiting the reduced power consumption state comprises storing the time of exiting in a register.

17. The method of claim 14 wherein the automatically calculating the reduced power consumption state duration is performed by the chip.

18. The method of claim 17 wherein the chip is a personal computer chipset.

19. The method of claim 14 wherein the reduced power consumption state is a C1 power state.

20. An apparatus comprising:

an operating system to read a time of entering a reduced power consumption state, and to read a time of exiting the reduced power consumption state prior to an execution of an interrupt routine; and

a main memory to store the time of entering.

21. The apparatus of claim 20 further comprising a chip to store the time of exiting the reduced power consumption state a register.

22. The apparatus of claim 20 further comprising a processor to store the time of exiting the reduced power consumption state in a register.

23. The apparatus of claim 21 wherein the chip is a personal computer chipset.

24. The apparatus of claim 21 wherein the operating system further operates to perform a cycle to the chip.

25. The apparatus of claim 20 wherein the operating system further operates to calculate a reduced power consumption state duration.

26. The apparatus of claim 20 wherein the reduced power consumption state is a C1 power state.

27. An apparatus comprising:

an operating system to request a chip to store a time of entering a reduced power consumption state and a time of exiting the reduced power consumption state; and

the chip to store the time of entering and the time of exiting the reduced power consumption state and to automatically calculate a reduced power consumption state duration.

28. The apparatus of claim 27 wherein the reduced power consumption state is a C1 power state.

29. The apparatus of claim 27 wherein the chip is a personal computer chipset.

30. An apparatus comprising:

an operating system to request a chip to start a time counter prior to entering a reduced power consumption state; and

the chip to start the time counter.

31. The apparatus of claim 30 wherein the operating system further operates to request the chip to halt the time counter.

32. The apparatus of claim 30 wherein the chip further operates to halt the time counter.

33. The apparatus of claim 30 wherein the time counter comprises a reduced power consumption state duration.

34. The apparatus of claim 30 wherein the chip is a personal computer chipset.

35. The apparatus of claim 30 where in the reduced power consumption state is a C1 power state.

36. An apparatus comprising:

means for reading a time of exiting a reduced power consumption state prior to an execution of an interrupt routine;

means for storing the time of exiting the reduced power consumption state in a register; and

means for calculating a reduced power consumption state duration.

37. The apparatus of claim 36 further comprising:

means for reading a time of entering the reduced power consumption state;

means for storing the time of entering the reduced power consumption state in a main memory; and

means for calculating the reduced power consumption state duration utilizing the time of entering and the time of exiting.

38. The apparatus of claim 36 wherein the reduced power consumption state is a C1 power state.

39. The apparatus of claim 36 wherein the register is located in a personal computer chipset.

40. The apparatus of claim 36 wherein the register is located in a processor.

41. An apparatus comprising:

means for starting a time counter;

means for entering a reduced power consumption state;

means for halting the time counter prior to an execution of an interrupt routine; and

means for exiting the reduced power consumption state.

42. The apparatus of claim 41 wherein the reduced power consumption state is a C1 power state.

43. The apparatus of claim 41 wherein the means for starting the time counter further comprise means for requesting a chip to start the time counter.

44. The apparatus of claim 41 wherein the means for halting the time counter further comprise means for requesting a chip to halt the time counter.

45. An apparatus comprising:

means for storing a time of entering a reduced power consumption state in a chip;

means for storing a time of exiting the reduced power consumption state in the chip prior to an execution of an interrupt routine; and

means for automatically calculating a reduced power consumption state duration.

46. The apparatus of claim 45 wherein the reduced power consumption state is a C1 power state.

47. The apparatus of claim 45 wherein the chip is a personal computer chipset.